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# UNITED STATES PATENT APPLICATION

# FOR

# ADHESIVE AND ENCAPSULATING MATERIAL WITH FLUXING PROPERTIES

## CROSS-REFERENCES TO RELATED APPLICATIONS

None

## STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH AND DEVELOPMENT

None

## INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC

None

## BACKGROUND OF THE INVENTION

This invention relates to electrical interconnection methods in electronic circuitry and more particularly to flip chip attachment and encapsulation of both naked semiconductors and chip scale packages (CSPs). The technology is commonly referred to as underfill technology.

## BACKGROUND ART

As is noted in US-A-5128746, solder bump interconnections when attaching chips to electronic circuitry eliminate the expense, performance limitations, low productivity and poor space utilization of wire bonding. As circuit density increases occur, while circuit board and assembly sizes continue to shrink, so-called flip-chip interconnection using solder bumps has proved to be the most suitable technique for satisfying such demands.

With the most common form of flip-chip interconnection, solder bumps are placed on terminals of the integrated circuit being produced while the substrate for the integrated circuit is still in the form of a small wafer or die. Commonly, the eutectic Sn/Pb 60/40 or a high melting alloy such as Sn/Pb 3/97, which is known to have been employed in the IBM C4 process, is employed as solder material. The die or wafer